

Please amend the claims as follows (this listing replaces all prior listings)

1 – 18. (cancelled).

19. (Currently amended) A method of generating a time signal comprising:

initializing a set of control signals;

generating a system time signal using a real time clock circuit that has a tunable oscillator for adjusting an operation frequency of the real time clock circuit, the tunable oscillator having a set of MOSFET-capacitors that can be independently selected based on the set of control signals;

receiving a reference time signal over a network; and

after the initializing, adjusting a set of the set of control signals to modify a selection of a subset of the MOSFET-capacitors in the tunable oscillator to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal.

20 – 27. (cancelled).

28. (Cancelled) The method of claim 19, further comprising biasing the MOSFET capacitors so that the selected MOSFET capacitors each has a specified capacitance.

29. (Cancelled) The method of claim 28, further comprising generating the control signals by using a logic circuit, and decoupling the capacitors from the logic circuit to prevent noise in the logic circuit from affecting the capacitors.

30. (Cancelled) The method of claim 29, further comprising generating a filtered voltage signal to power a buffer circuitry that decouples the capacitors from the logic circuit.

31. (Cancelled) The method of claim 30 in which biasing the MOSFET capacitors comprises using the filtered voltage signal to bias the MOSFET capacitors.

32. (Cancelled) The method of claim 19 in which the tunable oscillator comprises a resonator.

33. (Cancelled) The method of claim 32 in which modifying a selection of a subset of the MOSFET capacitors comprises using a subset of transmission gates to connect the selected MOSFET capacitors to the resonator.

34. (Cancelled) The method of claim 33, further comprising generating the control signals by using a logic circuit, and decoupling the transmission gates from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors through the transmission gates.

35. (Currently amended) An apparatus comprising:  
MOSFET capacitors, each selectable through an independent control signal generated by a logic circuit, the selected capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors;

a storage to store values for initializing the logic circuit;

a real time clock to generate an oscillating signal having a frequency dependent on the amount of capacitance provided by the selected MOSFET capacitors; and

~~a data processor to generate a system time signal based on the oscillating signal, to receive a reference time signal, and to control the logic circuit to select a different subset of the MOSFET capacitors to increase or decrease the frequency of the oscillating signal in response to a difference between the system time signal and the reference time signal~~

a data processor to generate an initial system time signal, receive a reference time signal, and generate an adjusted time signal,

in which the initial system time signal is derived from the oscillating signal generated by the real time clock using a subset of capacitors selected by the logic circuit initialized according to the values retrieved from the storage, and  
the adjusted time signal is generated by selecting a different subset of the capacitors to increase or decrease the frequency of the oscillating signal in response to a difference between the initial system time signal and the reference time signal.

36. (Currently amended) The apparatus of ~~claim 35~~ claim 37, further comprising a low pass filter connected to a DC voltage supply to provide a filtered voltage signal to bias the drains and sources of the MOSFET capacitors.

37. (Currently amended) The apparatus of ~~claim 36~~ claim 35 in which the ~~MOSFET capacitors comprise P-type enhancement mode MOSFETs~~ drain-source connected MOSFET capacitors.

38. (Currently amended) The apparatus of ~~claim 36~~ claim 37, further comprising buffer devices to decouple the MOSFET capacitors from the logic circuit to prevent noise in the logic circuit from affecting the capacitors.

39. (Currently amended) The apparatus of ~~claim 38, in which the filtered voltage signal is used~~ further comprising a low pass filter connected to a DC voltage supply to provide a filtered voltage signal to power the buffer devices.

40. (Cancelled) The apparatus of claim 35 in which the real time clock comprises a resonator coupled to the selected ~~MOSFET~~ capacitors.

41. (Currently amended) The apparatus of ~~claim 40~~ claim 35, further comprising transmission gates, each corresponding to one of the ~~MOSFET~~-capacitors, to couple the selected capacitors to the resonator.

42. (Previously presented) The apparatus of claim 41, further comprising buffer devices to decouple the transmission gates from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors through the transmission gates.

43. (Currently amended) The apparatus of claim 35 in which the ~~MOSFET~~-capacitors comprise drain-source connected P-type MOSFET capacitors.

44. (Previously presented) The apparatus of claim 35 in which at least one of the ~~MOSFET~~-capacitors has a capacitance that is less than 1 pF.

45. (Currently amended) The apparatus of claim 35 in which each capacitor comprises an N-type ~~depletion mode~~-MOSFET.

46. (Cancelled) The apparatus of claim 45 in which the real time clock comprises a resonator coupled to the selected capacitors.

47. (New) An electronic device, comprising:  
a real time clock to generate an oscillating signal having a frequency dependent on an amount of capacitance provided by a subset of capacitors selected from a set of capacitors;  
a basic input/output system (BIOS) having values for initializing the real time clock by selecting a first subset of capacitors; and  
a data processor to generate an initial system time signal, receive a reference time signal, and generate an adjusted time signal, in which the initial system time signal is generated based on the oscillating signal generated by the real time clock initialized according to the values

stored in the BIOS, and the adjusted time signal is generated by selecting a second subset of the capacitors to increase or decrease the frequency of the oscillating signal in response to a difference between the initial system time signal and the reference time signal.

48. (New) The electronic device of claim 47, comprising a register that stores a value indicating whether to initialize the real time clock based on the values in the BIOS after the electronic device is rebooted.

49. (New) The electronic device of claim 48 in which the BIOS evaluates the value stored in the register to determine whether to initialize the real time clock based on values in the BIOS.

50. (New) The electronic device of claim 47, comprising a non-volatile storage to store values representing the second subset of the capacitors.

51. (New) The method of claim 19, in which the capacitors comprise drain-source connected P-type MOSFET capacitors.

52. (New) The method of claim 51, further comprising using a low pass filter to generate a bias voltage to bias the drains and sources of the P-type MOSFET capacitors.

53. (New) The method of claim 19 in which initializing the set of control signals comprises initializing the set of control signals based on values stored in a basic input/output system (BIOS).

54. (New) The method of claim 53, comprising setting a flag to indicate whether, after rebooting of an electronic device that includes the real time clock, the set of control signals need to be initialized.

55. (New) The method of claim 54, further comprising, after rebooting the electronic device and initializing the set of control signals, setting the flag to indicate that the control signals do not need to be initialized the next time the electronic device is rebooted.